IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently amended) A digitally controlled oscillator, comprising:

an analog [[a]] preconditioner, wherein the analog preconditioner is operable to receive ~~receives~~ an input clock signal ~~, wherein the preconditioner receives~~ and a master clock signal, wherein the analog preconditioner is configured to output ~~outputs~~ a modified clock signal that is synchronized to the master clock signal, wherein the analog preconditioner is configured to noise shape phase noise of the synchronization to higher frequencies; and

a digital phase locked loop coupled to receive the modified clock signal output from the analog preconditioner, wherein the digital phase locked loop is also operable to receive ~~receives~~ the master clock signal, wherein the digital phase locked loop is configured to output ~~outputs~~ an output clock signal, wherein the output clock signal is a version of the input clock signal synchronized to the master clock signal [[;]]

~~wherein the digital phase locked loop does not introduce phase noise to the synchronized version of the input clock signal~~.

2. (Currently amended) The digitally controlled oscillator of claim 1,

~~wherein the preconditioner operates to noise shape phase noise of the synchronization to higher frequencies;~~

wherein the digital phase locked loop ~~operates~~ is configured to remove the phase noise at the higher frequencies.

3. (Currently amended) The digitally controlled oscillator of claim 2,

wherein the analog preconditioner has a higher bandwidth than the digital PLL.

4. (Currently amended) The digitally controlled oscillator of claim 1,

wherein the analog preconditioner includes a loop having a loop gain, wherein the loop gain operates to attenuate phase noise introduced internal to the analog preconditioner.

5. (Currently amended) The digitally controlled oscillator of claim 1, wherein the analog preconditioner comprises:

a phase detector including a first input which is operable to receive ~~receives~~ the input clock signal and a second input, wherein the phase detector also includes an output;

a loop filter ~~having~~ including an input coupled to the output of the phase detector and also including an output;

a voltage controlled oscillator (VCO) ~~having~~ including an input coupled to the output of the loop filter and also including an output;

a latch ~~having~~ including an input coupled to the output of the VCO, an input which is operable to receive ~~receives~~ the master clock signal, and also including an output which is operable to generate ~~generates~~ the modified clock signal, wherein the latch is configured to synchronize ~~synchronizes~~ the modified clock signal to the master clock signal, wherein the output of the latch is coupled to the second input of the phase detector to provide the modified clock signal to the phase detector.

6. (New) The digitally controlled oscillator of claim 5,

wherein the analog preconditioner is configured to noise shape phase noise of the VCO to higher frequencies.